

CLAIMS

1. A test board de-embedding method to improve RF measurements accuracy on an automatic testing equipment for IC wafers, wherein each wafer includes a device under test located on a wafer die plane and being contacted by probecard needles of a probecard that is coupled to a configuration board through a probe interface board, the method including the following phases:

performing an automatic calibration phase of said testing equipment up to an internal plane inside said automatic testing equipment;

performing a calibration plane transfer up to a plane of said configuration board;

performing a test boards de-embedding phase up to the wafer die plane.

2. The method according to claim 1, wherein said calibration plane transfer is performed by using a predetermined number of calibration standard loads on said wafer.

3. The method according to claim 1, wherein said calibration plane transfer is performed by using at least three calibration standard loads on said wafer.

4. The method according to claim 2, wherein said calibration standard loads are coaxial OSL (Open, Short, Load) standards.

5. The method according to claim 2, wherein said test boards de-embedding phase is performed using the same calibration standards realized on said wafer.

6. The method according to claim 2, said calibration standards have been realized directly using the pad portions of the integrated device realized on said wafer.

7. The method according to claim 2, wherein said used loads are: Open circuit, Short circuit and a 50 Ohm load, thus forming OSL (Open, Short, Load) calibration standards.

8. The method according to claim 2, wherein said calibration standards are defined on said wafer providing specific metal levels masks and a passivation mask for the device under test.

9. The method according to claim 1, wherein said probecard and said probe interface board depend on the device under test.

10. A method to improve RF measurements accuracy on an automatic testing equipment for IC wafers by implementing a test board de-embedding phase, wherein each wafer includes a device under test located on a wafer die plane and being contacted by probecard needles of a probecard that is coupled to a configuration board through a probe interface board, the method including the following phases:

performing an automatic calibration phase of said testing equipment up to an internal plane located inside said automatic testing equipment;

performing a calibration plane transfer up to a plane of said configuration board using a predetermined number of calibration standard loads realized on said wafer;

performing a test boards de-embedding phase up to the wafer die plane.

11. The method according to claim 10, wherein said calibration standard loads on said wafer are at least three.

12. The method according to claim 10, wherein said calibration standard loads are coaxial OSL (Open, Short, Load) standards.

13. The method according to claim 10, wherein said test boards de-embedding phase is performed using the same calibration standards realized on said wafer.

14. The method according to claim 10, said calibration standards have been realized directly using the pad portions of the integrated device realized on said wafer.

15. The method according to claim 10, wherein said loads used are: Open circuit, Short circuit and a 50 Ohm load, thus forming OSL (Open, Short, Load) calibration standards.

16. The method according to claim 10, wherein said calibration standards are defined on said wafer providing specific metal levels masks and a passivation mask for the device under test.

17. The method according to claim 10, wherein said probecard and said probe interface board depend on the device under test.

18. A method to improve RF measurements accuracy on an automatic testing equipment for IC wafers including at least a device or circuit under test located on a wafer die plane, the wafer being contacted by probecard needles of a probecard that is coupled to a configuration board of said equipment through a probe interface board, the method including the following phases:

performing a calibration phase of said testing equipment up to an internal plane located inside said automatic testing equipment;

performing a calibration plane transfer up to a plane of said configuration board using a predetermined number of calibration standard loads realized on said wafer;

performing a test boards de-embedding phase up to the wafer die plane.

19. The method according to claim 18, wherein at least three calibration standard loads on said wafer are used for said calibration plane transfer.

20. The method according to claim 18, wherein said calibration standard loads are coaxial OSL (Open, Short, Load) standards.

21. The method according to claim 18, wherein said test boards de-embedding phase is performed using the same calibration standards realized on said wafer.

22. The method according to claim 18, said calibration standards have been realized directly using the pad portions of the integrated device realized on said wafer.

23. The method according to claim 18, wherein said used loads are: Open circuit, Short circuit and a 50 Ohm load, thus forming OSL (Open, Short, Load) calibration standards.

24. The method according to claim 18, wherein said calibration standards are defined on said wafer providing specific metal levels masks and a passivation mask for the device under test.

25. The method according to claim 18, wherein said probecard and said probe interface board depend on the device under test.